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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/734,388	12/11/2000	John V.W. Reynders	P5431	4232

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EXAMINER	
KANG, INSUN	

ART UNIT	PAPER NUMBER
2124	5

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/734,388	REYNDERS, JOHN V.W.	
	Examiner	Art Unit	
	Insun Kang	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 April 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The priority date for the application is 12/11/2000.

2. This action is responding to application papers dated 12/11/2000, 2/26/2001, and 4/12/2001.

3. Claims 1-24 are pending.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick (US 6,106,575) and further in view of Ball (US 5,615,357).

-- In regard to claims 1, 11, and 21-24, Hardwick shows the self-tuning vector objects for optimization on parallel computers since vectors have well-established semantics and are suitable for divide and merge operations (Hardwick, col 12 lines 14-31, col 17 lines 1-67). Hardwick discloses various automated tuning functions associated with the vector objects using optimization techniques such as divide and merge and dynamic load balancing (Hardwick, col 17 lines 1-50, col 29 lines 23-67, col 30 lines 1-52, and col 37 lines 5-50).

Hardwick shows a method for receiving a user program (Hardwick, col 4 lines 64-67, and col 5 lines 1-7), but doesn't specifically show a method comprising simulating execution of said user program.

Simulations are used for discovering design errors, optimizing or fine-tuning a system, evaluating system performance, or simply better understanding a complex system through analysis. Ball specifically shows execution-driven simulators (Ball, col 2 lines 30-60) for the purpose of accurately evaluating performance of processor designs and detecting design errors.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ball to the method of Hardwick.

The modification would be obvious because simulating the execution of a program rapidly detects potential bottlenecks and hidden problems/weaknesses in a program design so that costly delays and errors can be minimized by more accurate forecasts and estimates before actual execution.

Hardwick discloses a method comprising detecting a plurality of expressions...in said user program (Hardwick, col 3 lines 47-56, col 6 lines 41-59, col 8 lines 33-57, and col 10 lines 32-40). Hardwick shows data-flow analysis and flow of control through program statements executed in a sequential order implying the trace files are generated reflecting the execution flow of the program (Hardwick, col 6 lines 46-54 and col 32 lines 44-61) but he doesn't specifically mention about dividing the trace file into blocks during simulation (Hardwick, col 3 lines 47-56, col 4 lines 56-63, and col 6 lines 46-59).

Ball discloses a trace file indicating a sequence of expressions divided into a plurality of trace file blocks, so that data dependencies between trace blocks are

minimized, execution time is shorten, network locality is maximized, and latency is lowered due to fewer hops between processors (Ball, col 2 lines 30-60, col 3 lines 14-25, col 6 lines 30-51, col 8 lines 7-67, col 9 lines 1-65, and col 7 lines 40-54).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Ball to the method of Hardwick. The modification would be obvious because dividing trace file into a plurality of trace file blocks can reduce data dependencies and greater network locality of processors can be achieved.

Hardwick discloses converting said trace file blocks into source code expression blocks (Hardwick, col 8 lines 15-30), generating a plurality of minimal timing (Hardwick, col 12 lines 1-13, col 10 lines 32-54, and col 11 lines 41-55), compiled expression blocks, each of said plurality of minimal timing, compiled expression blocks corresponding to a respective one of said source code expression blocks, said generating said plurality of minimal timing, compiled expression blocks including application of at least one compiler optimization technique (Hardwick, col 12 lines 5-6, 56-63, col 14 lines 52-63, cl 15 lines 10-19, col 13, col 14, and col 16 lines 1-19), and linking said plurality of minimal timing, compiled expression blocks into said user program (Hardwick, col4 lines 32-63, and col 16 lines 1-19).

-- In regard to claims 2 and 12, Hardwick inherently discloses detecting a plurality of expressions including said self-tuning object in said user program is performed by program code associated with at least one overloaded operator associated with said

self-tuning object (Hardwick, col 6 lines 4-59). Most of the arithmetic and relational operators are overloaded to work on arrays, which perform the specified operation on the elements of the array. Some of the mathematics functions are also overloaded to take array operands. The matrix and vector are basic classes in linear algebra computation. Hardwick discloses the data type vector for implemention of the parallel model that would be associated in data parallelism that would result in successive execution of functions using the overloaded operator (Hardwick, col 12 lines 25-31) to provide an easy to use interface, reasonable time and space efficiency. See col 10 lines 41-53, col 6 lines 41-col 7 lines 2, and col 15 lines 51-57.

-- In regard to claims 3 and13, see the rejection of claim 2 above.

--In regard to claims 4 and 14, Hardwick discloses that dividing trace file into plurality of trace file blocks is performed such that a total amount of computational dependencies and synchronization requirements within said user program, including computational dependencies and synchronization requirements between trace file blocks are minimized (Hardwick, col 5 lines 2-8, lines 39-49, col 10 lines 10-54, col 11 lines 14-18, col 25 lines 28-40 col 27 lines 2-10, and col 14 lines 27-46).

-- In regard to claims 5 and 15, Hardwick shows C functions delimited by curly braces in a program. For example, see col 19 lines 15-35. However, Hardwick doesn't specifically disclose that dividing said trace file into said plurality of trace file blocks is performed responsive to user provided delimiters included within said user program.

Ball shows that the trace file is generated for data/execution flow analysis containing a sequence of program instructions. Ball discloses by dividing trace files into trace file blocks, more accurate performance statistics can be obtained in a relatively short time by running a relatively small portion of a program (Ball, col 8 lines 38-65) and minimize the data/execution analysis complexity.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Ball to the method of Hardwick. The modification would be obvious because dividing trace file into a plurality of trace file blocks is performed responsive to user provided delimiters included within said user program so that the execution flow analysis complexity can be reduced and more accurate performance statistics can be more quickly obtained.

-- In regard to claims 6 and 16, Hardwick discloses that generating plurality of minimal timing, compiled expression blocks further comprises compiling and executing at least one of expression blocks multiple times while varying a value of at least one optimization parameter for said at least one compiler optimization technique (Hardwick, col 12 lines 56-63).

-- In regard to claims 7 and 17, Hardwick discloses that said generating said plurality of minimal timing, ...further comprises timing multiple executions of compiled expression blocks (Hardwick, col 13 lines 1-16, and col 10 lines 32-40).

-- In regard to claims 8 and 18, Hardwick discloses that linking of minimal timing compiled expression blocks to user program is responsive to execution of user program (Hardwick, col 16-lines 1-19, and col 4 lines 32-38).

-- In regard to claims 9 and 19, Hardwick discloses that detecting during execution of user program, plurality of expressions including self-tuning object in user program (Hardwick, col 16 lines 1-19, and col 10 lines 32-40).

-- In regard to claims 10 and 20, Hardwick discloses scheduling minimal timing compiled expression blocks for execution on at least one processor of target parallel processing computer (Hardwick, col 10 lines 32-54, and col 32 lines 34-43).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 703-305-6465. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 703-305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-0000.

IK

10/10/2003

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124